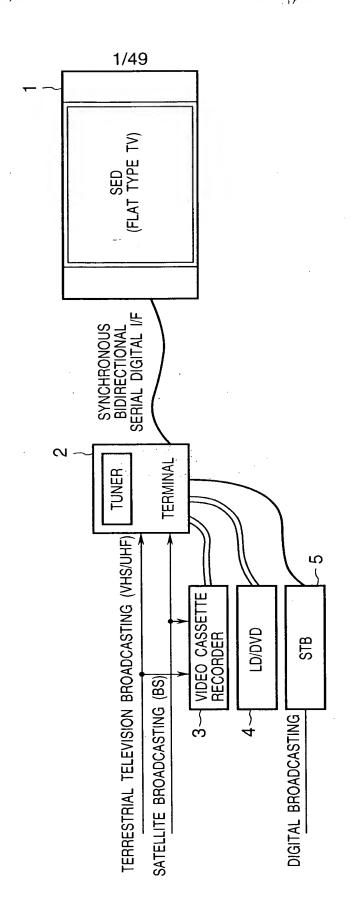
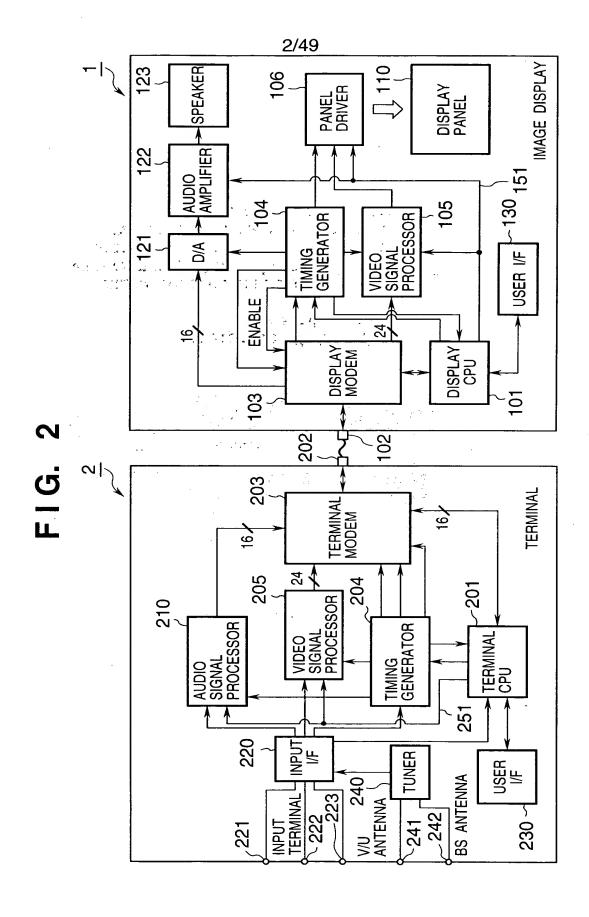
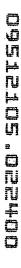
<u>Т</u>

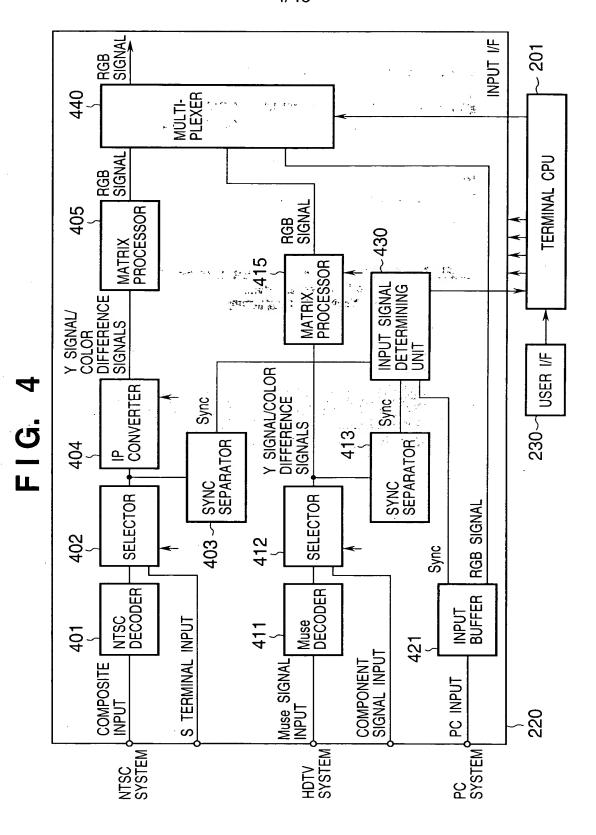


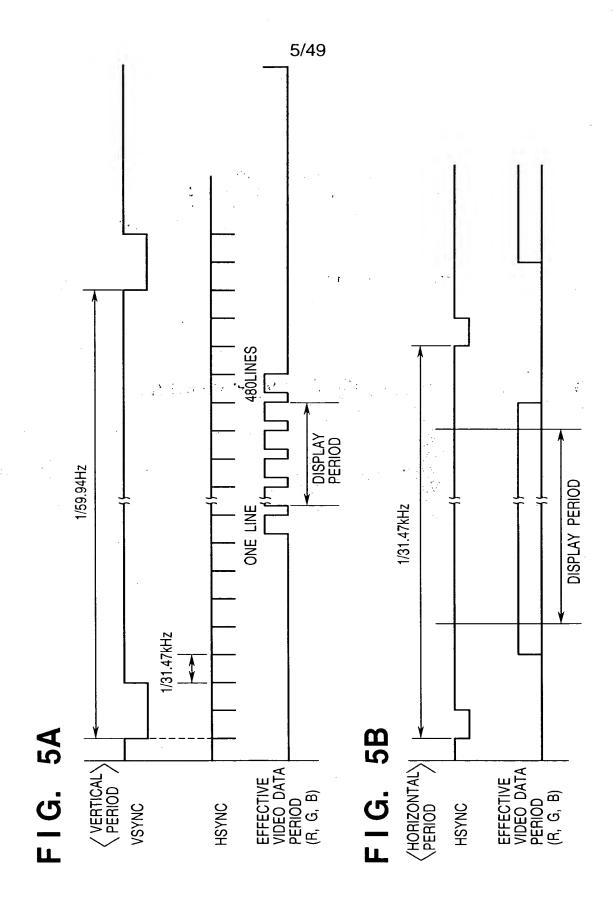


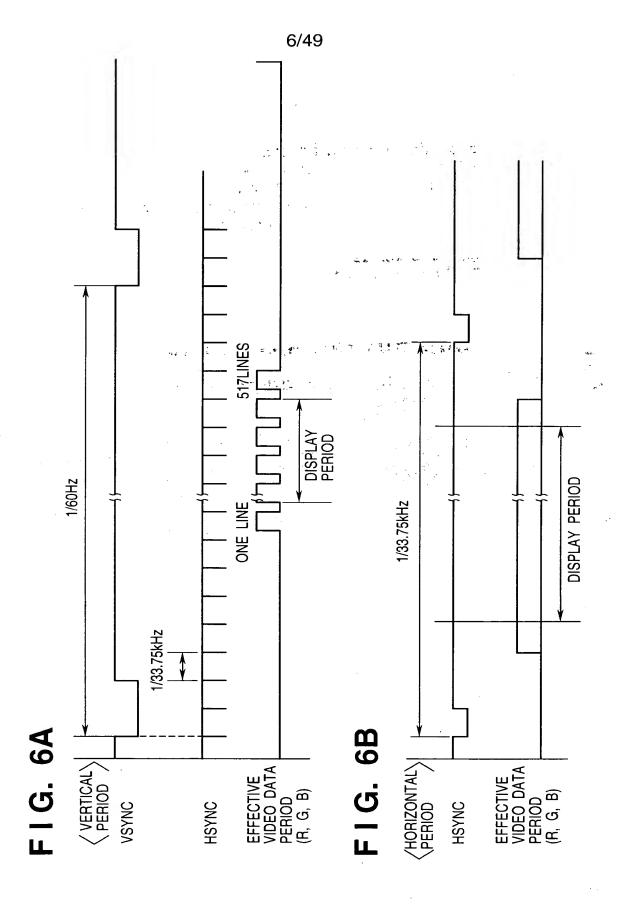
اراتين مارو

3/49 COMMUNI-CATION DIRECTION CONTROL TIMING SYNC • REGEN-RATION DISPLAY CPU command 9 24 DEMULTI PLEXER 101 314 24 16 DISPLAY MODEM 312 313, DEMODU-LATOR MODU-LATOR 311 310 103 |||||||| 203 411 TERMINAL MODEM 320 -TRANSMISSION TIMING RECEPTION TIMING 322 DEMODU-LATOR MODU-LATOR SYNCHRO-NIZATION _ 321 PC LINE 24(16)
Sommand Harring S4 L 324 9 DATA BUS TERMINAL CPU 323 24 COMMUNI-CATION DIRECTION CONTROL ACOUSTIC— SIGNAL TIMING CONTROL⁻ VIDEO SIGNAL-

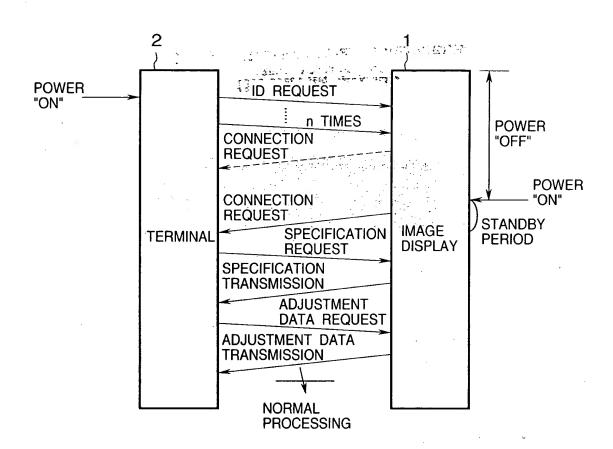


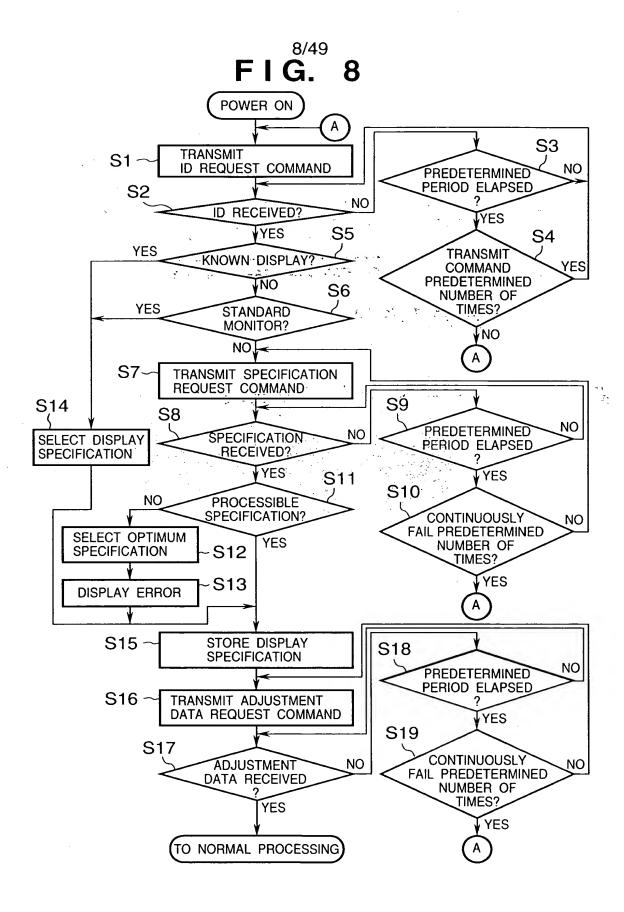




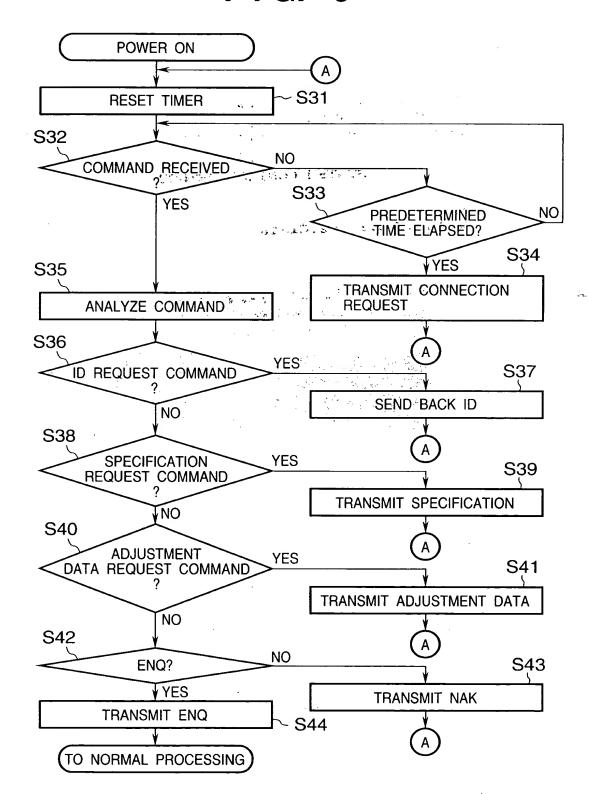


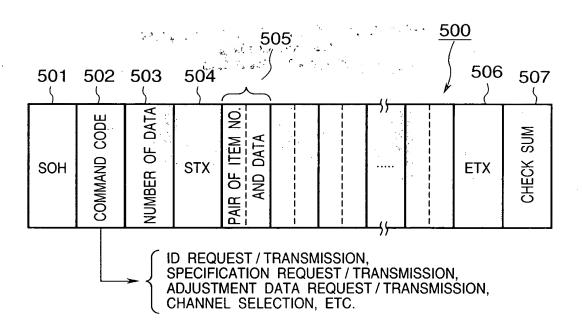
i ji i

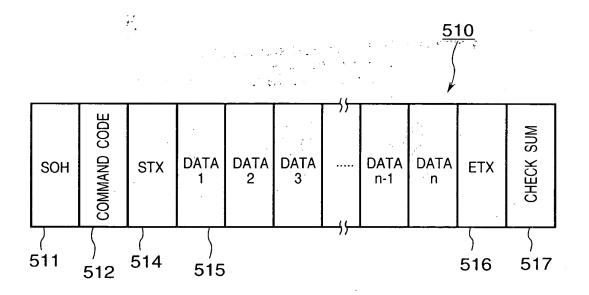


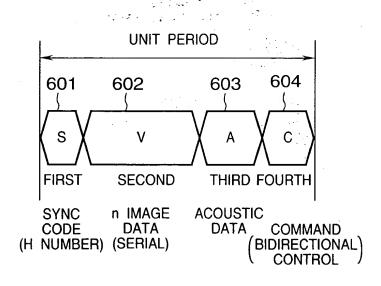


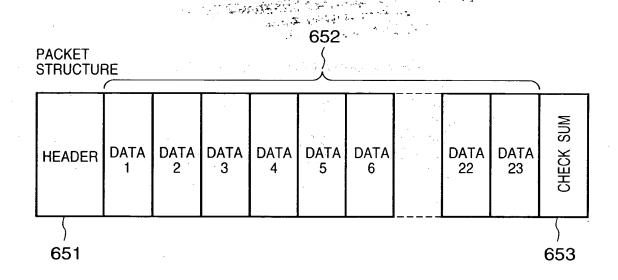
9/49 **FIG. 9**









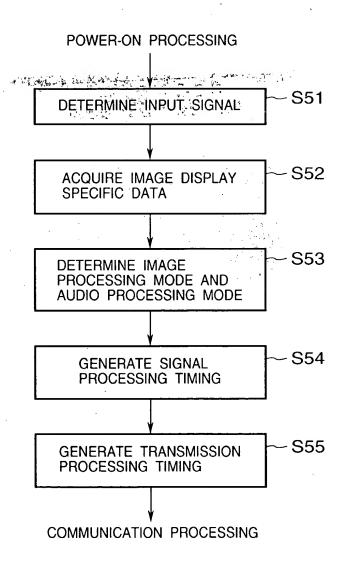


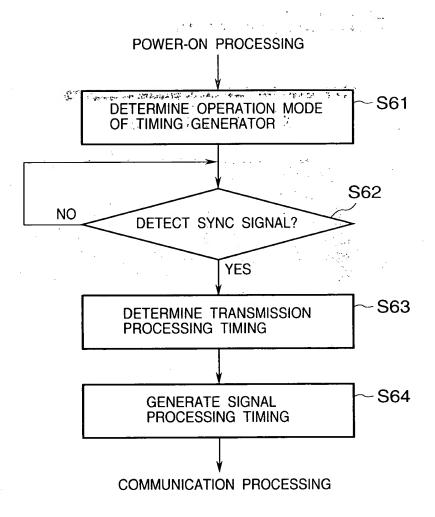
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FIG. 14A

FIG. 14B

DISPLAY→TERMINAL		TERMINAL → DISPLAY	
HEADER DATA 1		DATA 1	
2	DISPLAY TYPE 13 19	:]:	RECEPTION SIGNAL TYPE 1
3	DISPLAY TYPE 2	3	RECEPTION SIGNAL TYPE 2
4	DISPLAY TYPE 3	4	RECEPTION SIGNAL TYPE 3
5	COMMAND 1 (ADJUSTMENT MODE)	5	COMMAND 1 (ADJUSTMENT MODE)
6	COMMAND 2 (ADJUSTMENT RIGHT)	6	COMMAND 2 (ADJUSTMENT RIGHT)
7	CONTRAST	7	CONTRAST
8	COLOR TEMPERATURE 1 (G_LEVEL) ******	8	COLOR TEMPERATURE 1
9	COLOR TEMPERATURE 2- (B_LEVEL)	9	COLOR TEMPERATURE 2 (B_LEVEL)
10	COLOR TEMPERATURE 3 (R_LEVEL)	10	COLOR TEMPERATURE 3 (R_LEVEL)
11	BRIGHTNESS	11 '	BRIGHTNESS
12	G_Black LEVEL	12	G_Black LEVEL
13	B_Black LEVEL	13	B_Black LEVEL
14	R_Black LEVEL	14	R_Black LEVEL
15	GAMMA / G_GAMMA	15	GAMMA / G_GAMMA
16	B_GAMMA / R_GAMMA	16	B_GAMMA / R_GAMMA
17	DISPLAY MODE	17	DISPLAY MODE
18	HORIZONTAL / VERTICAL DISPLAY SIZE	18	HORIZONTAL / VERTICAL DISPLAY SIZE
19	HORIZONTAL / VERTICAL DISPLAY POSITION	19	HORIZONTAL / VERTICAL DISPLAY POSITION
20	VOLUME	20	VOLUME
21	VOLUME L & R BALANCE	21	VOLUME L & R BALANCE
22	DISPLAY AUDIO SPECIFICATION	22	
23		23	
	CHECK SUM		CHECK SUM





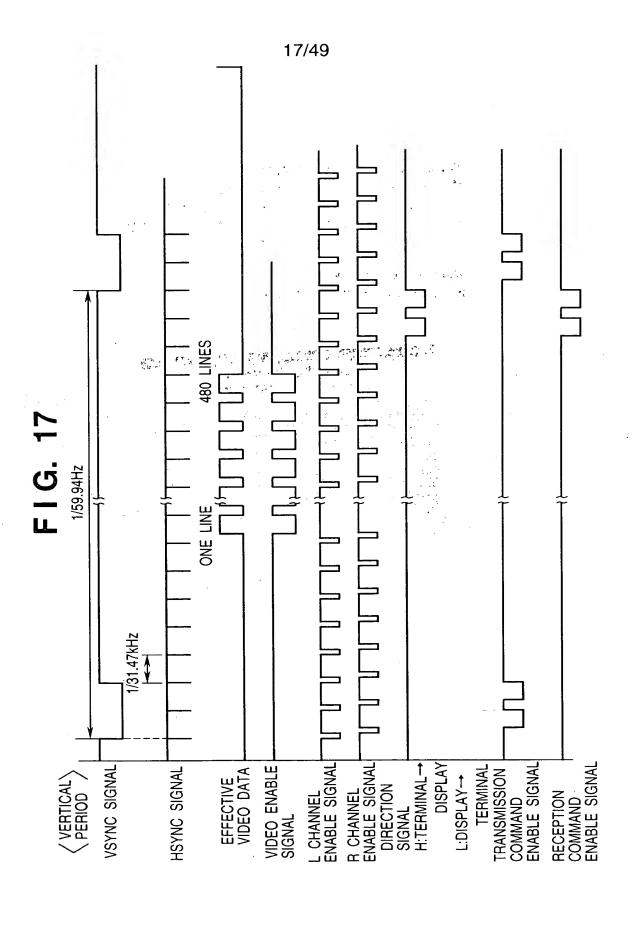
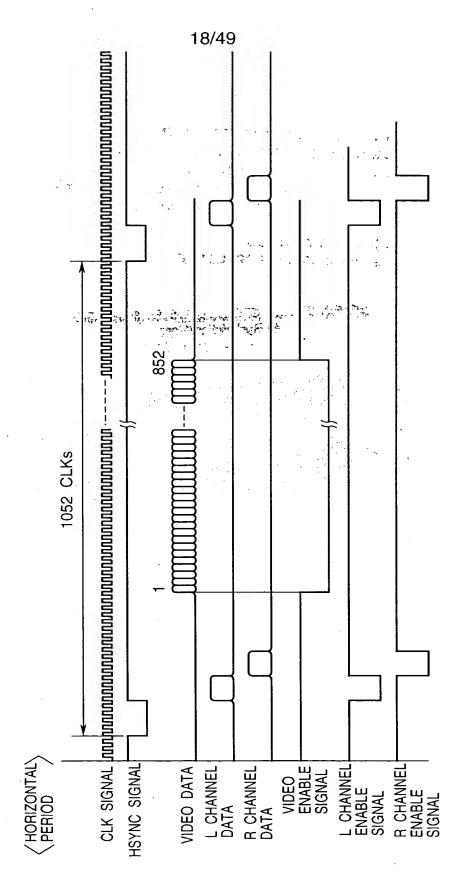


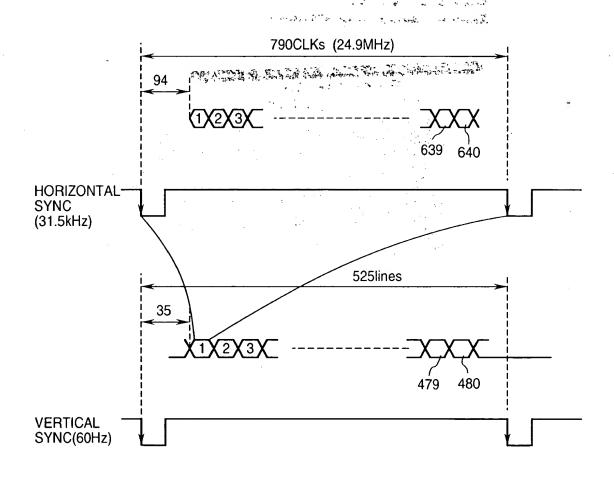
FIG. 18



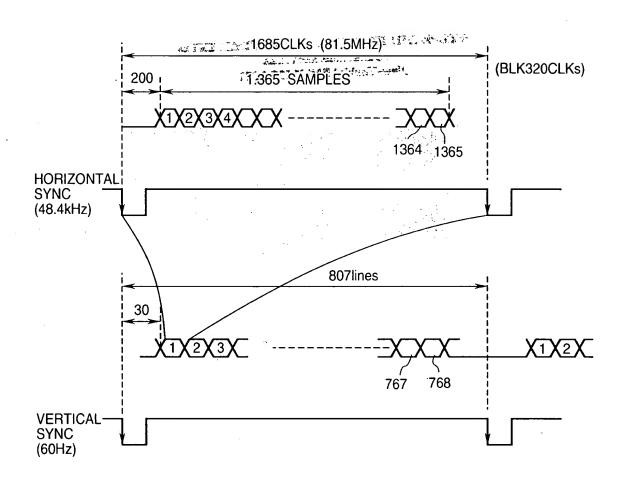
851 852 479 480 1052CLKs (33.1MHz) 525lines 125 35 HORIZONTAL SYNC (31.5kHz) VIDEO DATA

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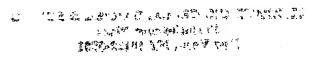
. .

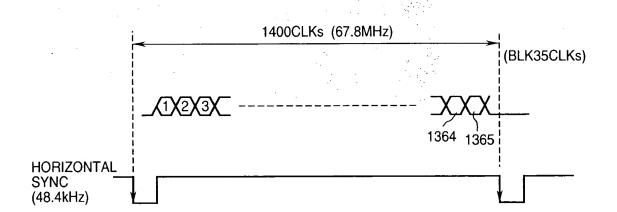


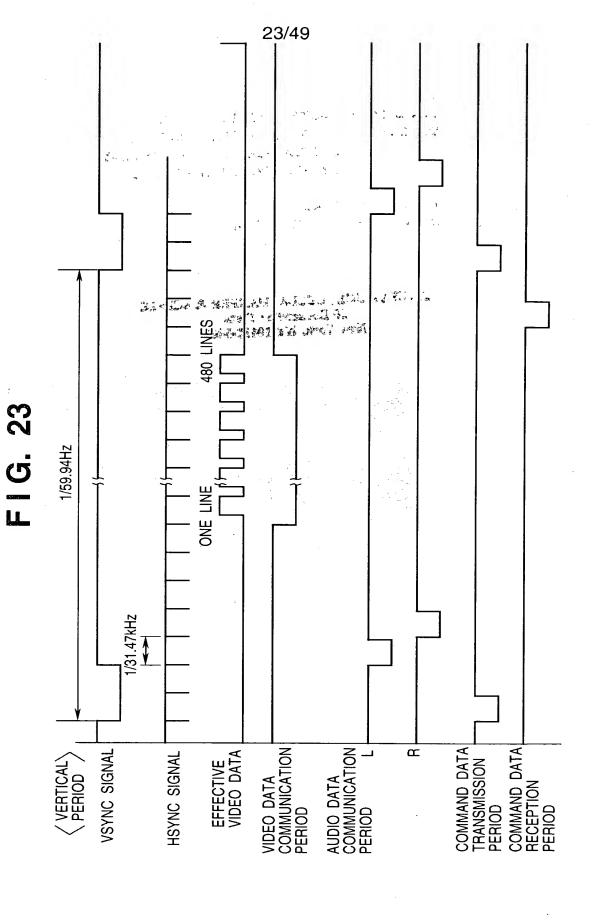
F I G. 21



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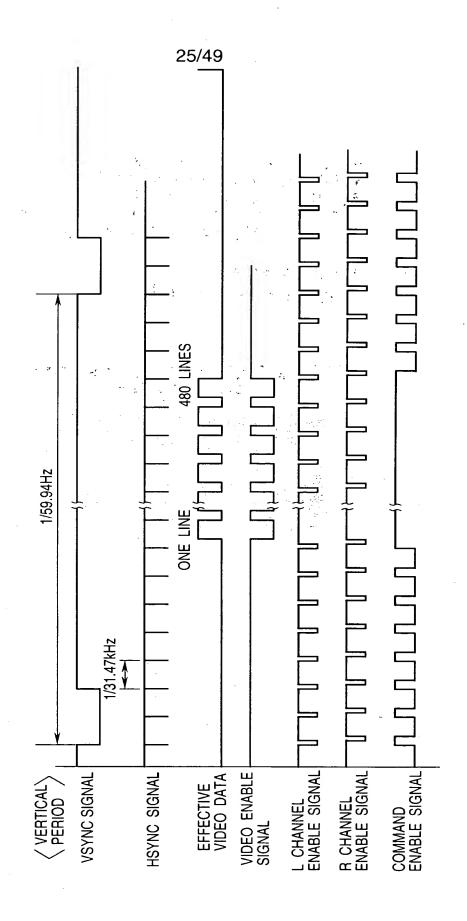


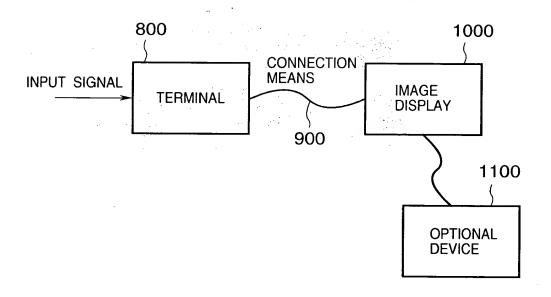


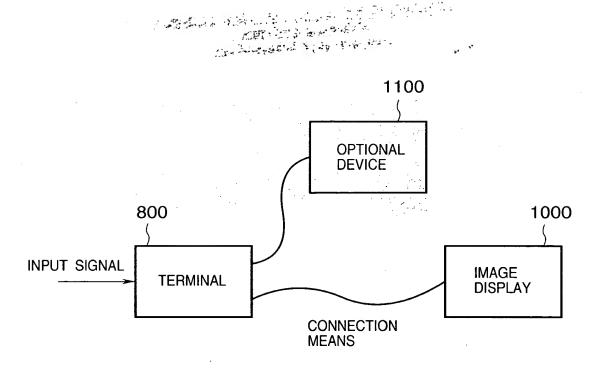
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FIG. 25







28/49 1100 OPTIONAL DEVICE 123 1000 SPEAKER 110 106 PANEL DRIVER ~ 130 DISPLAY PANEL EXTERNAL INPUT/ TERMINAL 122 AUDIO AMA PLIFIER USER | 654 ~ 105 **652** 653 D/A VIDEO SIGNAL PROCESSOR EXTERNAL TIMING GENERATOR GENERATOR EXTERNAL I/F 121~ 104 TIMING 1* \$\frac{1}{2} \tag{1} 京 林 弘 IMAGE DISPLAY EXTERNAL MODEM DISPLAY MODEM DISPLAY CPU FIG. 28 651 5 103 655 900 203 TERMINAL MODEM A TERMINAL TERMINAL MODEM B TERMINA 20 ₹ 609 √ 602 GENERATOR SIGNAL PROCESSOR TIMING GENERATOR B ۸ D ⋖ 601 \sim 909 608 607 **SELECTOR** 220 OPTIONAL INPUT 44 TERMINAL INPUT I/F EXTERNAL OUTPUT TERMINAL 609 USER I/F 800 230

4

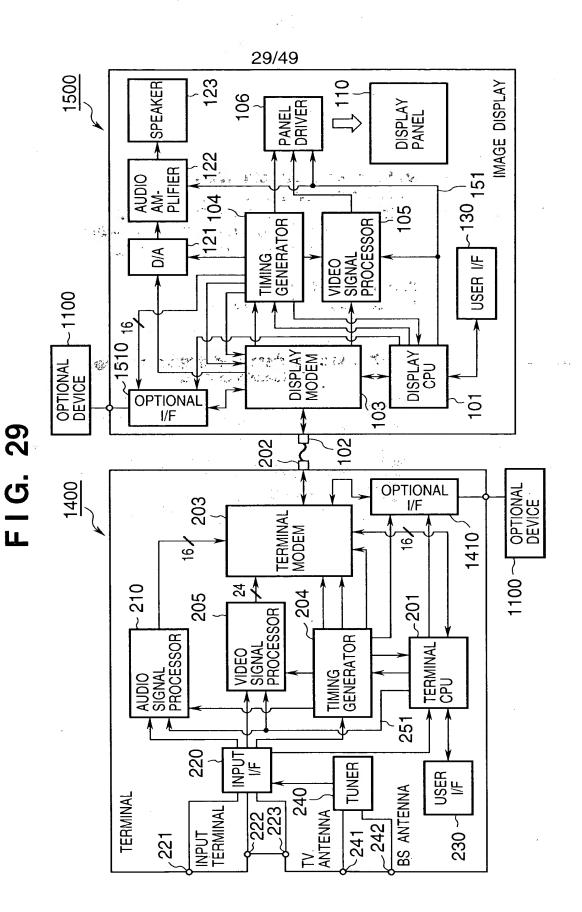
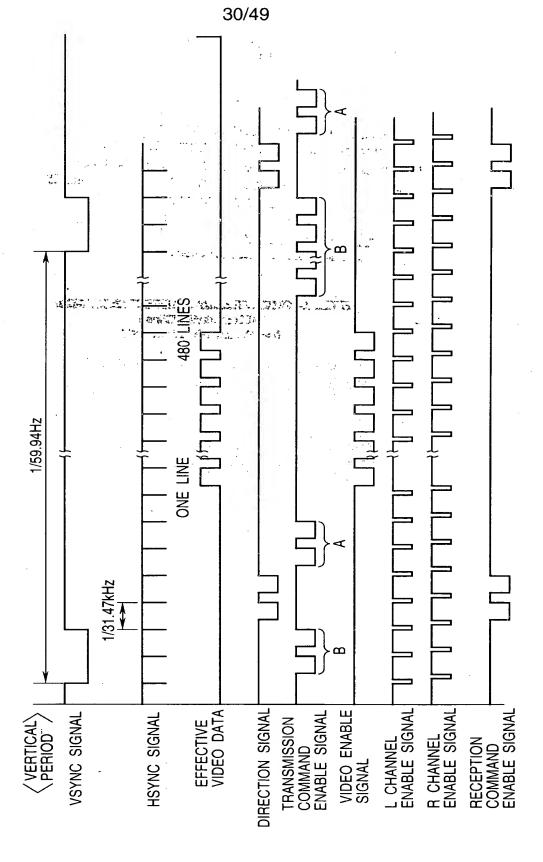
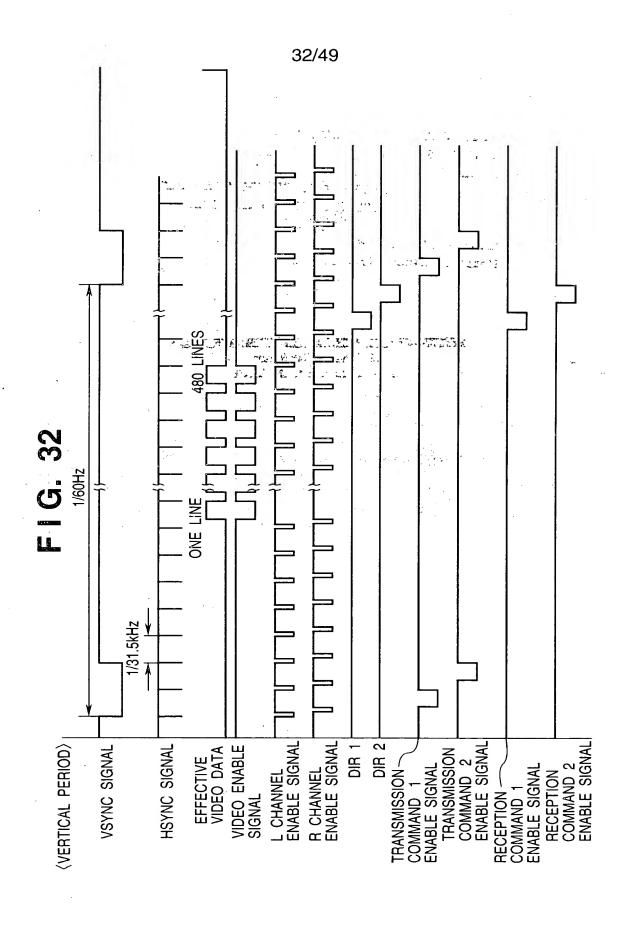


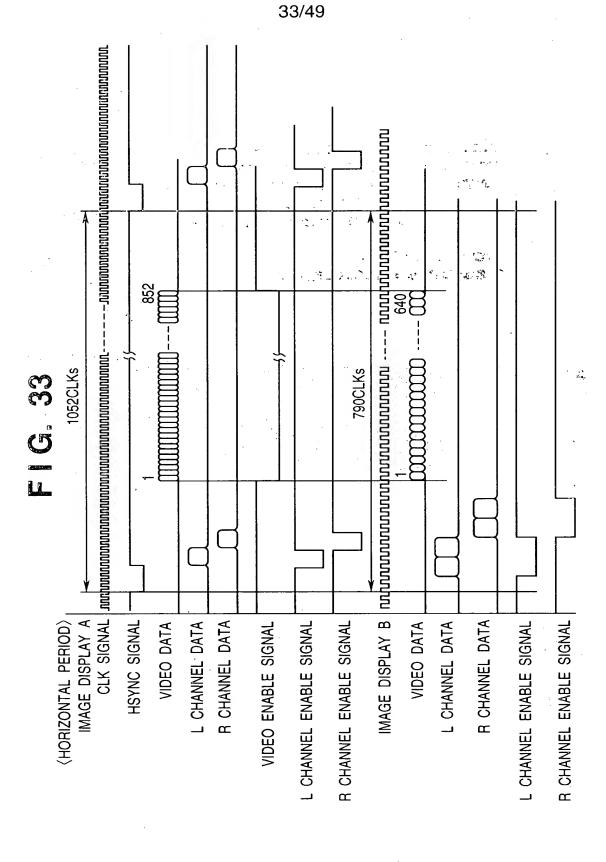
FIG. 30

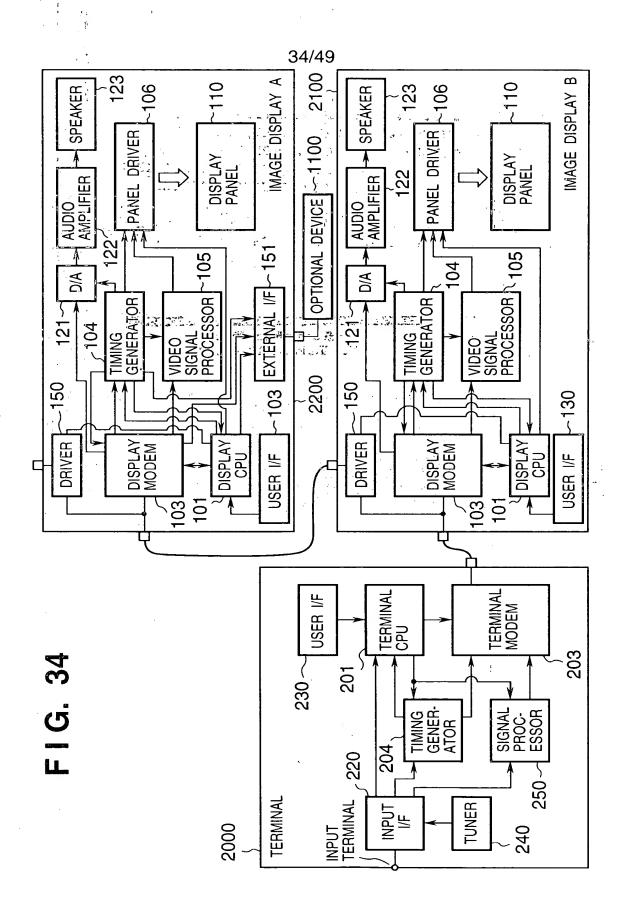


in i

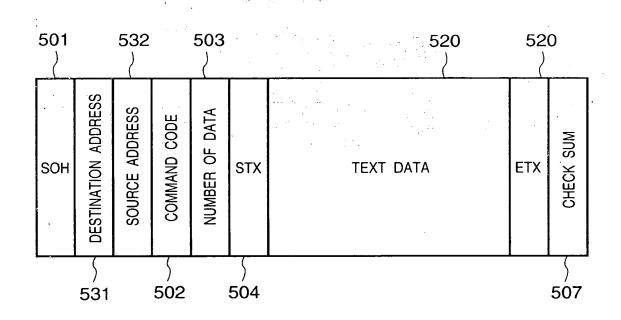
31/49 123 SPEAKER PANEL DRIVER DISPLAY PANEL 106 122 AUDIÓ AMPLIFIER 104 IMAGE DISPLAY B $^{-103}$ -Ÿ .. VIDEO SIGNAL PROCESSOR GENERATOR Ø O USER 121~ DISPLAY CPU DISPLAY MODEM ⋖ IMAGE DISPLAY 103 T C C 1800l 1700 1603 1602 1601 TERMINAL MODEM B TERMINAL MODEM A TERMINAL CPU SIGNAL PROCESSOR A TIMING GENERATOR A TIMING GENERATOR B SIGNAL PROCESSOR B 1604 1607 1606 1605 1 220 240 INPUT I/F USER I/F TUNER INPUT TERMINAL TERMINAL 1600 230



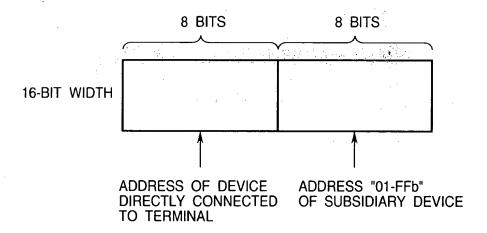


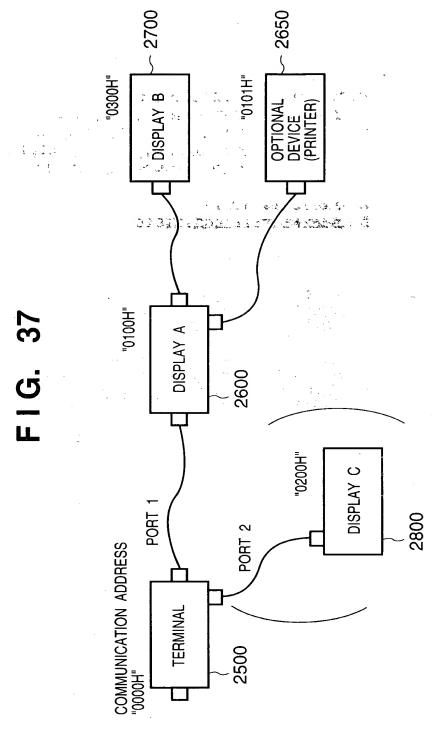


- F.I.G. 35



F.I.G. 36

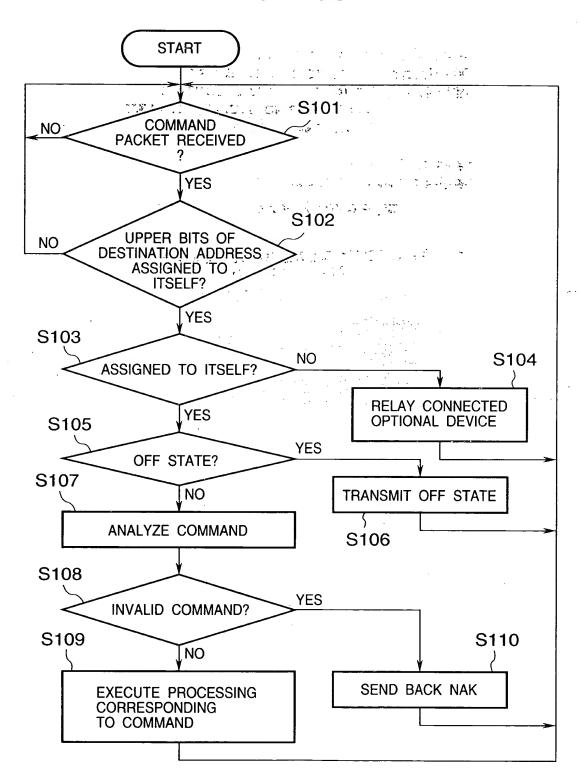




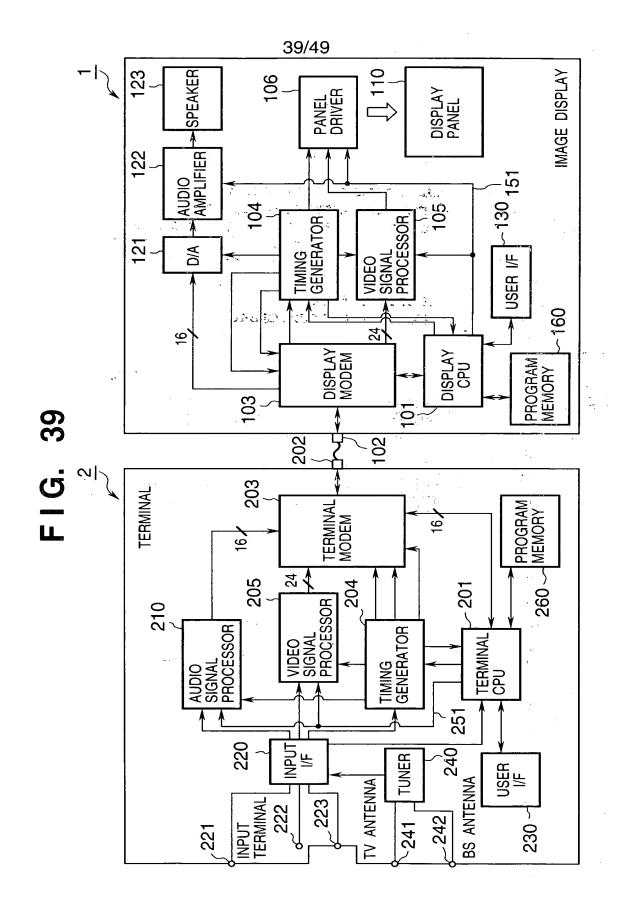
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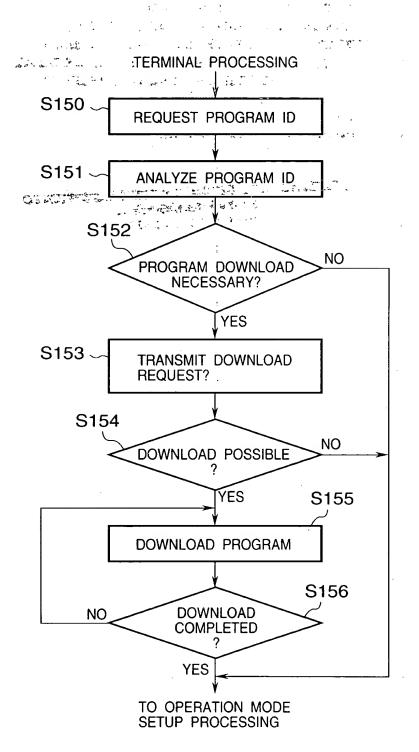
FIG. 38



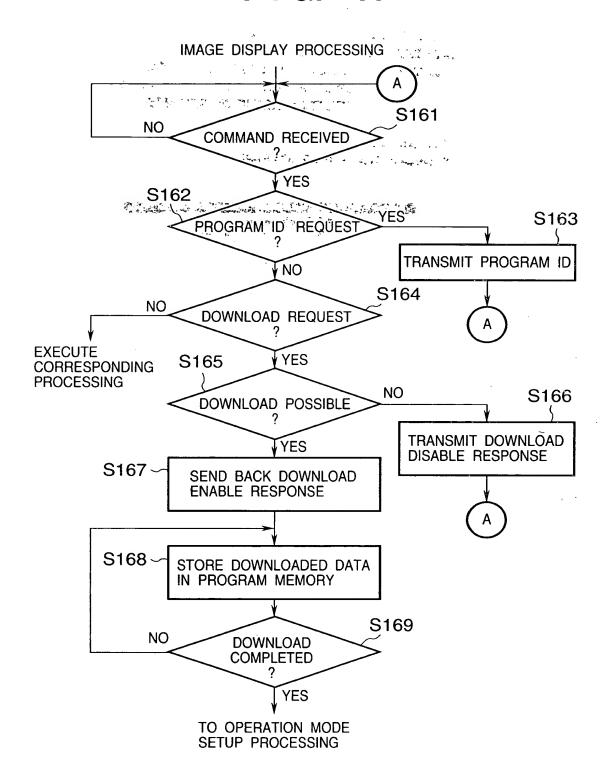
3



1 × 1 × 1



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122 AUDIO AMPLIFIER 104 -103 7 IMAGE DISPLAY B VIDEO SIGNAL PROCESSOR GENERATOR USER I/F D/A TIMING **121**² 5 DISPLAY MODEM DISPLAY CPU ⋖ IMAGE DISPLAY 103 FIG. 42 172 1800 171 271 1700 ~ 1603 1601 1602 TERMINAL MODEM B TERMINAL MODEM A TERMINAL CPU TIMING GENERATOR A 1604 SIGNAL PROCESSOR A $\boldsymbol{\omega}$ TIMING GENERATOR B SIGNAL PROCESSOR F 1607 1606 1605 ~1 220 240 INPUT I/F USER I/F TUNER **TERMINAL** TERMINAL 1600 INPUT 230

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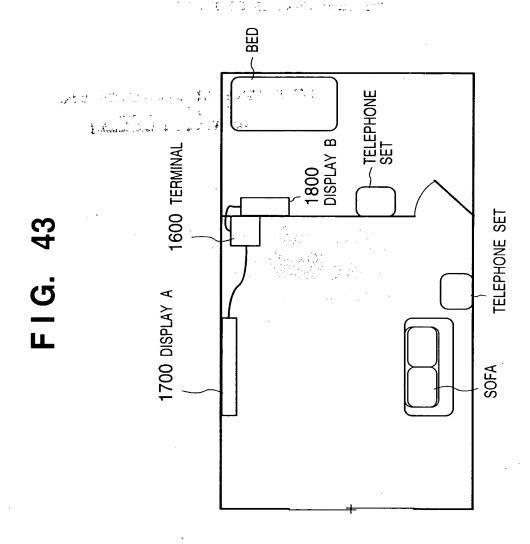
DISPLAY PANEL

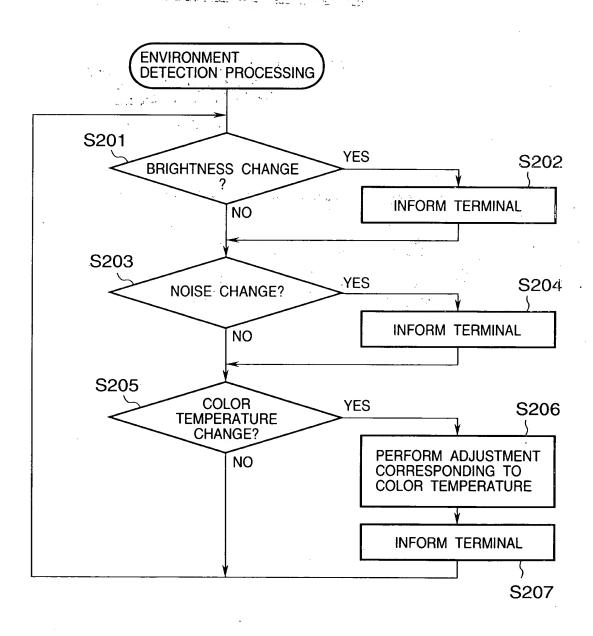
123

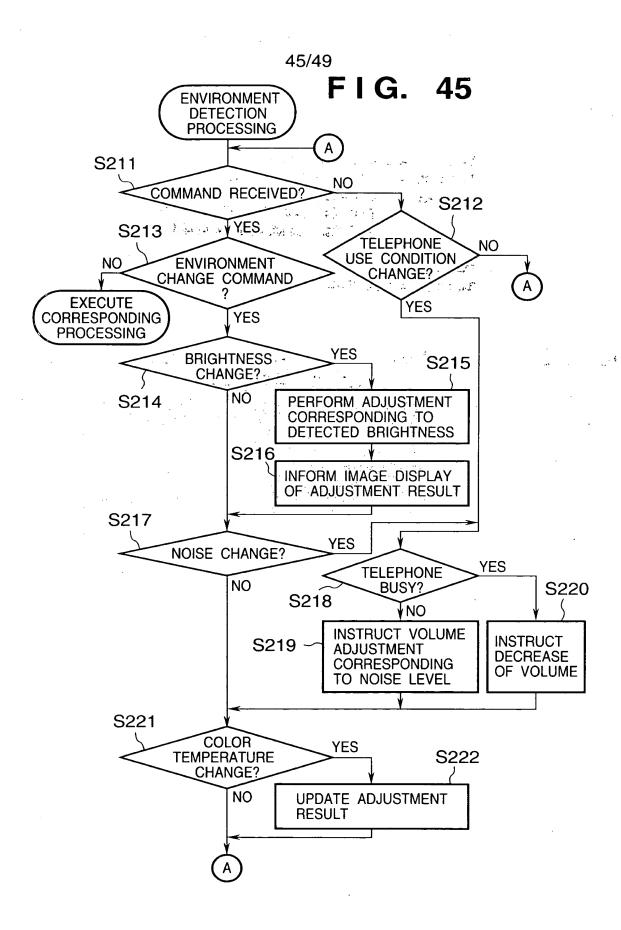
SPEAKER

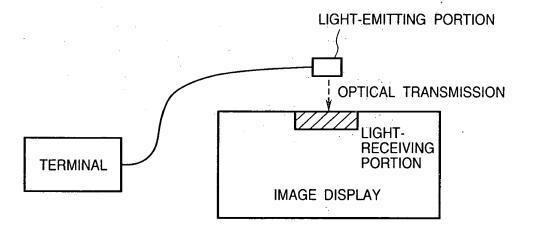
. 901

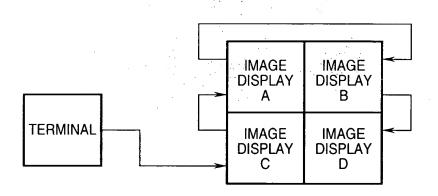
PÁNEL DRIVER

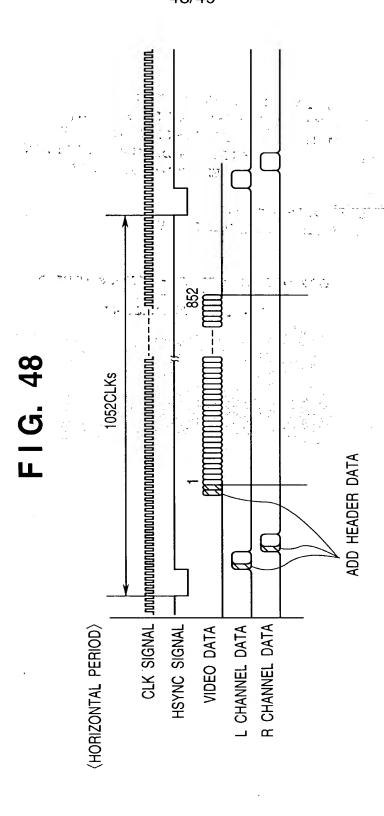












7.8

FIG. 49 PRIOR ART

